IN THE CLAIMS

Please amend the claims as follows:

Claims 1-9 (Canceled).

Claim 10 (Original) A method of manufacturing a nonvolatile semiconductor memory having a memory cell area in which memory cell transistors are formed and a peripheral circuit area in which peripheral transistors are formed, comprising:

forming a first insulating film over the entire surface of a semiconductor substrate;

forming a first electrode layer over the entire surface of the first insulating film;

selectively removing the first electrode layer, the first insulating film and the semiconductor substrate;

forming device isolation regions to self-align to the first electrode layer;

etching the device isolation regions until the top of the device isolation regions in the memory cell area reaches a level midway between the surface of the first electrode layer and the surface of the first insulating film;

forming a second insulating film over the entire surface of the semiconductor substrate;

removing a portion of the second insulating film over each of the peripheral transistors of the peripheral circuit area to form an opening that exposes a portion of the first electrode layer;

forming a second electrode layer over the entire surface of the semiconductor substrate;

forming a gate masking pattern on the second electrode layer;

patterning the second electrode layer using the gate masking pattern as a mask;

selectively etching away the second insulating film using the gate masking pattern as a mask;

etching the device isolation regions in the memory cell area until their top reaches the same level as the top of the first insulating film;

etching the device isolation regions in the peripheral circuit area until their top reaches a level midway between the surface of the first electrode layer and the surface of the first insulating film; and

selectively etching away the first electrode layer using the gate masking pattern as a mask.

Claim 11 (Original) The method according to claim 10, wherein, in the memory cell area, the first and second electrode layers form the floating gate and the control gate, respectively, of each of the memory cell transistors, and, in the peripheral circuit area, the first and second electrode layers form the gate of each of the peripheral transistors.

Claim 12 (Original) A method of manufacturing a nonvolatile semiconductor memory having a memory cell area in which memory cell transistors are formed and a peripheral circuit area in which peripheral transistors are formed, comprising:

forming a first insulating film over the entire surface of a semiconductor substrate;

forming a first electrode layer over the entire surface of the first insulating film;

selectively removing the first electrode layer, the first insulating film and the semiconductor substrate;

forming device isolation regions to self-align to the first electrode layer;

etching the device isolation regions until the top of the device isolation regions in the memory cell area reaches a level midway between the surface of the first electrode layer and the surface of the first insulating film;

forming a second insulating film over the entire surface of the semiconductor substrate;

removing a portion of the second insulating film over each of the peripheral transistors of the peripheral circuit area to form an opening that exposes a portion of the underlying first electrode layer;

forming a second electrode layer over the entire surface of the semiconductor substrate;

forming a gate masking pattern on the second electrode layer;

patterning the second electrode layer using the gate masking pattern as a mask so that its portion is left over the device isolation regions in the memory cell area;

selectively etching away the second insulating film using the gate masking pattern as a mask and the underlying patterned second electrode layer;

etching the device isolation regions in the peripheral circuit cell area until their top reaches a level midway between the surface of the first electrode layer and the surface of the first insulating film;

etching the second electrode layer and the first electrode layer using the gate masking pattern as a mask under etching conditions of high selectivity to the second insulating film until the top of the first electrode layer reaches a level below the surface of the second insulating film in the memory cell area;

selectively etching away the second insulating film;

etching the device isolation regions until their top reaches the same level as the surface of the first insulating film; and

etching the first electrode layer using the gate masking pattern as a mask under etching conditions of high selectivity to the first insulating film to form stacked gates each of which is comprised of the first electrode of one-layer structure and the second electrode layer.

Claim 13 (Original) A method of manufacturing a nonvolatile semiconductor memory having a memory cell area in which memory cell transistors are formed and a peripheral circuit area in which peripheral transistors are formed, comprising:

forming a first insulating film over the entire surface of a semiconductor substrate;

forming a first floating gate electrode layer over the entire surface of the first insulating film;

selectively removing the first floating gate electrode layer, the first insulating film and the semiconductor substrate;

forming device isolation regions to self-align to the first electrode layer, the top of the device isolation regions being at the same level as the surface of the first floating gate electrode layer;

forming a second floating gate electrode layer on the first floating gate electrode layer;

forming a control gate electrode layer over the entire surface of the semiconductor substrate;

forming a gate masking pattern on the control electrode layer;

patterning the control electrode layer using the gate masking pattern as a mask;

etching away the second insulating film using the gate masking pattern as a mask;

etching away the second floating gate electrode layer using the gate masking pattern as a mask;

etching the first floating gate electrode layer until its top reaches a level midway between the top of the device isolation regions and the surface of the first insulating film;

etching the device isolation regions using the gate masking pattern as a mask until their top reaches the same level as the surface of the first insulating film; and

etching away the remainder of the first floating electrode layer using the gate masking pattern as a mask.

Claim 14 (New) The method according to claim 12, wherein, in the memory cell area, the first and second electrode layers form the floating gate and the control gate, respectively, of each of the memory cell transistors, and, in the peripheral circuit area, the first and second electrode layers form the gate of each of the peripheral transistors.